



ISC0501: 1024x1024 2-Color QWIP ROIC

Specification

November 20, 2006

INDIGO OPERATIONS DOCUMENT # 400-0501-09 VERSION 1.00

This Presentation Contains Information Proprietary to FLIR Systems Corporation



Revision History

- **Version 1.00, November 20, 2006**
 - Initial Release



ROIC Description (1 of 2)

- **Design high performance 2 color CMOS ROIC for QWIP detectors**
 - 1024 x 1024 for each color
 - Shared unitcell, 30um pixel pitch
 - Die size Goal of $X < 35\text{mm}$ $Y < 39\text{mm}$
 - Designed for QWIP detectors
 - Coincident detectors
 - Direct injection input circuit for each detector
 - Simultaneous integration for each detector
 - Variable integration time for each color
 - Snap shot integration – integrate then read out and integrate while readout
 - 60 Hz frame rate
 - Total well capacity $\geq 17 \times 10^6$ carriers
 - On chip skimming for dark current correction



ROIC Description (2 of 2)

- **Multiple operating modes controlled by serial data interface**
 - Adjustable detector bias for each color
 - On-chip selectable gain for each color
 - Adjustable internal bias supplies to control power dissipation



Preliminary MWIR and LWIR Detector Characteristics

Dual-band QWIP for air borne applications (ABL)

→ Low background

QWIP Parameter	Specification Requirement	Comments
MWIR Spectral Range	4.3 to 5.1 μm → peak \approx 4.7 μm	
MWIR Dark Current	0.1pA to 2pA	60 to 70K, Typical \sim 1.5pA
MWIR Detector Bias	\approx 2V	Up to 3V
MWIR R_{DET}	\approx $2 \times 10^7 \Omega \cdot \text{cm}^2$ (TBR)	(RoA)
MWIR DQE x Photodetection Gain	$\eta(\lambda) \cdot \text{gain} = 0.06$	Responsivity $R(\lambda) = (e/h\nu) \cdot \eta(\lambda) \cdot \text{gain}$
LWIR Spectral Range	8.0 to 9.0 μm → peak \approx 8.5 μm	
LWIR Dark Current	10pA to 100pA	60 to 70K, Typical \sim 50pA
LWIR Detector Bias	\approx 2V	Up to 3V
LWIR R_{DET}	\approx $7 \times 10^5 \Omega \cdot \text{cm}^2$ (TBR)	(RoA)
LWIR DQE x Photodetection Gain	$\eta(\lambda) \cdot \text{gain} = 0.03$	Responsivity $R(\lambda) = (e/h\nu) \cdot \eta(\lambda) \cdot \text{gain}$
Bonding Pads	3 bumps + Vdetcom Ring Around Array	V_{DETCOM} + 2 color outputs (3 bumps) + Vdetcom Ring Around Array
Charge Polarity (to ROIC)	Hole collection in ROIC	Charge collection
Temperature of Operation	60K to 70K	65K typical



ISC0501 Preliminary Specification and Requirements Review (1 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	1024 x 1024	Large-format
Pixel Size	30um x 30um	
Spectral Range	MWIR: 4.3-5.1um LWIR: 8-9um	Drives well capacity requirements
Input Polarity	Hole Collection	GaAs/AlGaAs QWIP detector
Input Configuration	Direct Injection (DI)	P-Channel Inputs
Detector Bias Uniformity	< 20mV 1- σ	Dependent on Process Vt Uniformity
Core Multiplexing Configuration	Voltage Mode	IWR & ITR
Detector Impedance	> 7.7x10 ¹⁰ Ohms (LWIR = Color B) > 2.2x10 ¹² Ohms (MWIR = Color A)	Used for Simulation
Detector Capacitance	≤30fF (LWIR) ≤100fF (MWIR)	Used for Simulation
Test Detector pads	4 Pads /Color to test individual detectors	
Input Biases (C4 process)	VPD 5.0V VND 0.0V VPOS 5.0V VNEG 0.0V VPOSOUT 5.0V VNEGOUT 0.0V VDETCOM 5.0-7V (TBR) VOSA,B 1.6-3.8V VREFA,B 1.5-1.7V VOUTREFA,B,[1-2] 1.5V-1.7V VTESTA,B 0.0-5.0V	Digital Positive Digital Return Analog Positive Analog Return, Substrate Bias Output Positive Output Return Detector Common Skimming Control (Adj) Analog Channel Reference (Adj) S/H Reference (Adj) Test Row Input (Adj)



ISC0501 Preliminary Specification and Requirements Review (2 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS										
Input Clocks	<table border="0"> <tr> <td>Name</td> <td>Vhigh to Vlow</td> </tr> <tr> <td>CLK</td> <td>VPD to VND</td> </tr> <tr> <td>FSYNC</td> <td>VPD to VND</td> </tr> <tr> <td>DATA</td> <td>VPD to VND</td> </tr> <tr> <td>RESET_B</td> <td>VPD to VND</td> </tr> </table>	Name	Vhigh to Vlow	CLK	VPD to VND	FSYNC	VPD to VND	DATA	VPD to VND	RESET_B	VPD to VND	Master Clock (5MHz) Frame Sync Serial Data Line Global Reset
Name	Vhigh to Vlow											
CLK	VPD to VND											
FSYNC	VPD to VND											
DATA	VPD to VND											
RESET_B	VPD to VND											
Input Clock Rise and Fall, Jitter	CLK: 2ns rise/fall, ± 0.5 ns jitter FSYNC, DATA: 20ns rise/fall	10% to 90% Preliminary (TBR)										
Number of Outputs	8 Analog per color	Additional 1 reference output/Color Voltage Mode Analog at 10MHz (8/Color+1Ref/Color=18 outputs total)										
Output Modes	4, and 8 Analog per color	Common Output Mode for each color										
Windowing	Row Only Windowing Minimum Window of 1 Rows											
Analog Output	1.6V to 3.6V (TBR)	Signal Outputs										
Analog Output Interface	> 100k Ohms // ≤ 20 pF	Design for Lower Capacitance, Can Optimize Mux Power Setting										
Analog Output Voltage Swing	≥ 2.0 V	VPOS=5V										
Analog Output Data Rate	10MHz	5MHz Master Clock										
Analog Output Settling Time	Settle to 0.1% in ≤ 65 ns	At Operating Temperature										



ISC0501 Preliminary Specification and Requirements Review (3 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Frame Rate (1024 x 1024)	60Hz (8 outputs per color)	ITR, IWR, Additional 1 reference output/color
Input Current Min Nominal Max	MWIR LWIR 0.1 pA 10 pA 7.5 pA 110 pA 1 nA 1nA	Simulation Range, Includes Dark Current
Total Well Capacity	$\geq 17 \times 10^6$ carriers	Unit Cell Layout Limited, Goal of 20×10^6 carriers
Well Capacity Ratio	4:1 (LWIR:MWIR)	Repartition can be accomplished with 1-3 layer mask change
Gain Control	2 Bits Adjustment	Separate for Each Color
Transimpedance Non-Linearity	$< \pm 0.5\%$ (20% to 90% of dynamic range)	Output Voltage vs. Tint (Vout – Best Fit) / Max Range
Noise	$\leq 420 e^-_{RMS}$ at $3.4 \times 10^6 e^-$ $\leq 1250 e^-_{RMS}$ at $13.6 \times 10^6 e^-$	MWIR (COLOR A) LWIR (COLOR B)
Power	$\leq 600mW$	Goal of $\leq 400mW$
Operating Temperature	60K - 77K Stability $< 0.1K$	ROIC Shall Meet All Specs Over This Range
Adjacent Pixel Crosstalk	$< 0.1\%$	
Non-Adjacent Pixel Crosstalk	$< 0.1\%$	
Color-Color Crosstalk	$< 0.1\%$	



ISC0501 Preliminary Specification and Requirements Review (4 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Control Register Functions	Programmable Test On-chip Bias Control (TBD) On-chip Gain Control* Detector Bias Adjustment* Integration Time* Integration Time Resolution* Row Windowing	See Command Definition * Per Color Y dimension windowing only
Detector Bias Adjust	5 Bits Adjustment ≥ 2V range	Internal Headroom and charge capacity limit detector bias range. Separate For Each Color, On-chip Detector Bias Adjustment Can Be Disabled for External Detector Bias
Anti Blooming Control	Yes	Internally Biased, Over Rides to Detector, Bias Adjust IG for Test Mode
Integration Mode	Snap Shot ITR & IWR	Integrate Both Colors Simultaneously
Integration Time Control	10 Bits Adjustment	Separate For Each Color
Skimming	Voltage Skimming Capability	Separate For Each Color Adjustable Through Pads
ROIC Dimensions	< 35mm x 39mm (TBR)	Stitched process, Layout modular
Detector Bond Pad Location	Two detector pads and det com pads per pixel. Det com pad ring outside cell array	
Temperature Sensor	0.7V +/- 0.05V @ 300K 1.070V +/- 0.05V at 78K	