



# **ISC0905: 640 x 512 30 $\mu$ m Two Color ROIC**

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## **Specification**

January 13, 2012



# ISC0905 Revision History

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- **Version 1.00: August 27, 2010**
  - Initial Release
- **Version 1.01: January 13, 2012**
  - Removed markings for public release



# ISC0905 Specification and Requirements Review (1 of 5)

ROIC PARAMETER	0905 SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	640 x 512	
Pixel Pitch in Columns	30 $\mu$ m	
Pixel Pitch in Rows	30 $\mu$ m	
Input Polarity	Selectable P-on-N (Current Flows into Inputs) & N-on-P (Current Flows out of Inputs)	Color Selectable on a Per frame basis SLS, InSb, InGaAs, HCT
Detector Bond Pad	1 (6 $\mu$ m x 6 $\mu$ m) pad opening per pixel plus detector common pad ring around cell array	One indium bump connection per pixel. Additional detector common pad ring of 6 pixels around the array of 640x512 for a total array of 652x524
Test Detector Pads	4 pads to test individual detectors	Maintain the similar pixel locations as the ISC9803
Input Configuration	Direct Injection (DI)	
Core Multiplexing Configuration	Voltage Mode	
Detector Impedance (RrAd) at 77K	> 1x10 <sup>3</sup> (Ohm-cm <sup>2</sup> )	Impedance at reverse bias operating point. Used for Performance Analysis, Prediction and Simulation



# ISC0905 Specification and Requirements Review (2 of 5)

ROIC PARAMETER	0905 SPECIFICATION REQUIREMENT	COMMENTS												
Detector Capacitance	$\leq 0.6\text{pF}$	Used for Performance Analysis, Prediction and Simulation Estimated												
Temperature of Operation	65K-300K	Room Temperature Operation Will Have Reduced Performance.												
Input Biases	VDETCOM 0-5.5V VPOS 5.5V VPOSOUT 5.5V VPD 5.5V  VOUTREF 1.55V - 4.7V VNEG 0.0V VNEGOUT 0.0V VND 0.0V	Detector Common (optional) Analog Positive Output Positive Digital Positive  Analog Reference; P-on-N 1.55V; N-on-P 4.7V Analog Negative Output Negative Digital Negative												
Input Clocks	<table border="1"> <thead> <tr> <th>Name</th> <th>Vhigh to Vlow</th> </tr> </thead> <tbody> <tr> <td>CLK</td> <td>VPD to VND</td> </tr> <tr> <td>LSYNC</td> <td>VPD to VND</td> </tr> <tr> <td>FSYNC</td> <td>VPD to VND</td> </tr> <tr> <td>DATA</td> <td>VPD to VND</td> </tr> <tr> <td>RESET_B</td> <td>VPD to VND</td> </tr> </tbody> </table>	Name	Vhigh to Vlow	CLK	VPD to VND	LSYNC	VPD to VND	FSYNC	VPD to VND	DATA	VPD to VND	RESET_B	VPD to VND	Master Clock Line Sync Frame Sync (Integ. Control) Mode Control Master Reset (optional)
Name	Vhigh to Vlow													
CLK	VPD to VND													
LSYNC	VPD to VND													
FSYNC	VPD to VND													
DATA	VPD to VND													
RESET_B	VPD to VND													
Input Clock: Rise and Fall	10% to 90% in 5nS													
Outputs	Selectable 4 or 8 with Reference Output													
Output Interface	$\geq 100\text{k Ohms}$ $\leq 12\text{ pF}$	12pF includes capacitive load up to and including wire-bond to ROIC pad												



# ISC0905 Specification and Requirements Review (3 of 5)

ROIC PARAMETER	0905 SPECIFICATION REQUIREMENT	COMMENTS
Output Voltage Swing	2.5V $\pm$ 0.2V (Baseline P-on-N $\sim$ 1.55V $\pm$ 0.1V) (Baseline N-on-P $\sim$ 4.7V $\pm$ 0.1V)	Default settings: $\sim$ 2.5V $\pm$ 0.2V typical output range at 77K Estimated range for 0.8V reverse detector bias Output swing dependent on reverse bias
Power	8 Outputs $\leq$ 330mW 4 Outputs $\leq$ 235mW	Full frame operation at 18MHz output data rate and T=77K
Control Register Functions	Programmable Test I/O Anti-Blooming Control Power Control Master Current Detector Bias Adj. Invert/Revert Windowing (programmable size and position) 4 or 8 Outputs Reference Output Enable Adjustable Timing Edges Global Reset Pixel Color Select	
Programmable Test	Test Row Input Unit Cell Test Injection VET Circuit	
Detector Bias Adjust (P on N)	0mV to -800mV Adjustment @ nominal current (1nA)	$\sim$ 8mV bit bias control per color
Detector Bias Adjust (N on P)	0mV to +800mV Adjustment @ nominal current (1nA)	$\sim$ 8mV bit bias control per color



# ISC0905 Specification and Requirements Review (4 of 5)

ROIC PARAMETER	0905 SPECIFICATION REQUIREMENT	COMMENTS
Detector Bias Uniformity	< 20mV 1- $\sigma$	Dependent on Process Vt Uniformity Measured ISC9705 1-sigma of approximately 7mV, expect similar performance from ISC0905
Integration Mode	Snap Shot ITR & IWR	Integrate one color per frame
Integration Time	> 100 $\mu$ s to 0.9*full frame Adjustable on a per frame basis	For 240HZ $\rightarrow$ 4.167ms full frame $\rightarrow$ 3.75ms max tint Lowest Tint estimated, it is possible to program Tint to <100 $\mu$ s, but integrated output may be nonlinear and limited.
Total Input Current Min Nominal Max	20pA 1 nA 10nA	Simulation Range, includes signal and dark current
Input Charge Handling	$\geq 18 \times 10^6$ carriers	Can reduce well size with minimal layer changes
Non-Linearity	< $\pm$ 2% from least squares line fit	Output Voltage vs. Tint Max deviation from least squares fit over 15% to 85% of full range
Noise	$\leq$ -80dB of Full Well (Input Referred) At Maximum Readout Rate	Without Detector or System Noise ROIC Noise in dB defined as $20 \cdot \log(\text{noise } e^- / \text{full well } e^-)$



# ISC0905 Specification and Requirements Review (5 of 5)

ROIC PARAMETER	0905 SPECIFICATION REQUIREMENT	COMMENTS
Column Output Order-8 Output A ⋮ Output H	Column 0,8,...,632 ⋮ Column 7,15,...,639	Eight Output Mode Normal Readout Direction
Invert / Revert	Reverse Order of Rows and/or Columns	Select using Control Register
Temperature Sensor	0.7V ± 0.05V @ 300K 1.070V ± 0.05V at 77K	Test/Temp Pad
Full Frame Rate Pixel Rate 18MHz & T=77K unless otherwise noted	8 Output ≥ 240 FPS 4 Output ≥ 120 FPS	9MHz ISC0905 input clock For 512x512 windowed array Warm operation will have slower frame rate
Data Valid / Settling Time	Settle to 0.1% @ T=77K in ≤ 45ns	12pF // 100kΩ load Default power settings; 10ns Data Valid Warm operation requires longer settling time
Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K < 1.0% @ T=300K	Limited routing and system impedance
Non-Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K 8 output < 1.0% @ T=300K 8 output	Limited routing and system impedance
Color-Color ROIC Pixel Crosstalk	< 0.1% @ T=77K < 1.0% @ T=300K	Limited routing and system impedance
Minimum Window Size and Resolution	≥ 32 columns x 8 Rows ≥ 64 columns x 8 Rows	4 Output Mode 8 Output Mode
Die Size	< 23mm x 21mm	To edge of scribe lane Die extent to fit within the extent of the reticle exposure area
Pad Layout	Maximizing commonality with ISC0903	Match with ISC0903 as much as practical given the array size